Docket No.: P2001,0241

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : JUDITH MAGET ET AL.

Filed : CONCURRENTLY HEREWITH

Title : INTEGRATED, TUNABLE CAPACITANCE DEVICE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

S i r :

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

U.S. Patent No. 6,172,378 B1 (Hull et al.), dated January 9, 2001;

U.S. Patent No. 5,965,912 (Stolfa et al.), dated October 12, 1999;

U.S. Patent No. 6,351,020 B1 (Tarabbia et al.), dated February 26, 2002;

U.S. Patent No. 6,034,388 (Brown et al.), dated March 7, 2000;

Patent Abstracts of Japan 03147376 A (Hidetomo), dated June 24, 1991;

European Patent Application EP 1 024 538 A1 (Manzini et al.), dated August 2, 2000;

Svelto, F. et al.: "A Three Terminal Varactor for RF IC's in Standard CMOS Technology", IEEE Transactions on Electron Devices, Vol. 47, No. 4, April 2000, pp. 893-895;

Castello, R. et al.: "A +-30% Tuning Range Varactor Compatible with future Scaled Technologies", IEEE, Symposium on VLSI Circuits Digest of Technical Papers, 1998, pp. 34-35;

Wong, W. M. Y. et al.: "A Wide Tuning Range Gated Varactor", IEEE Journal of Solid-State Circuits, Vol. 35, No. 5, May 2000, pp. 773-779;

Tiebout, M.: "A Fully Integrated 1.3GHz VCO for GSM in 0.25µm Standard CMOS with a Phasenoise of –142dBc/Hz at 3MHz Offset", European Microwave Week, 2000, 4 pages;

Andreani, P. et al.: "On the Use of MOS Varactors in RF VCO's", IEEE Journal of Solid-State Circuits, Brief Papers, Vol. 35, No. 6, June 2000, pp. 905-910;

Porret, A.-S. et al.: "Design of High-Q Varactors for Low-Power Wireless Applications Using a Standard CMOS Process", IEEE Journal of Solid-State Circuits, Vol. 35, No. 3, March 2000, pp. 337-345;

International Search Report, dated December 4, 2002.

Respectfully submitted,

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For Applicants

Date: October 3, 2003

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FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))	Attorney Docket No.: P2001,0241 Appl. No.: Applicant: JUDITH MAGET ET AL. Filing Date: October 3, 2003 Group Art Unit:

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A	6,172,378 B1	1/9/01	Hull et al.			
	B	5,965,912	10/12/99	Stolfa et al.			
	C	6,351,020 B1	2/26/02	Tarabbia et al.			
	D	6,034,388	3/7/00	Brown et al.			
	E						
	F						
	G						
	H						
	I						

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
	J	03147376 A	6/24/91	Japan				
	K	1 024 538 A1	8/2/00	Europe				
	L							
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

		Svelto, F. et al.: "A Three Terminal Varactor for RF IC's in Standard CMOS Technology", IEEE Transactions on Electron Devices, Vol. 47, No. 4, April 2000, pp. 893-895
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		Wong, W. M. Y. et al.: "A Wide Tuning Range Gated Varactor", IEEE Journal of Solid-State Circuits, Vol. 35, No. 5, May 2000, pp. 773-779
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		Porret, A.-S. et al.: "Design of High-Q Varactors for Low-Power Wireless Applications Using a Standard CMOS Process", IEEE Journal of Solid-State Circuits, Vol. 35, No. 3, March 2000, pp. 337-345

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